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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,963	01/22/2002	Aron T. Lunde	37829.0400	5214

20322 7590 08/16/2006

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 08/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,963	LUNDE, ARON T.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Applicant's Amendment

1. The non-final rejection as set forth in paper No. (041006) mailed on April 13th, 2006 is withdrawn in response to Applicants' amendments. A new rejection is made as set forth in this Office Action. Claims (1-28) are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Higgins, III (U.S. Patent 5,378,981).

In re claim 1, **Higgins** discloses a method for preparing a die on a wafer for testing by a testing apparatus, the method comprising, forming a die 30 on a wafer 10, the die having an active portion 20 comprising integrated circuitry, wherein the die 30 has a plurality of input bond pads 34 formed on the active portion 20;

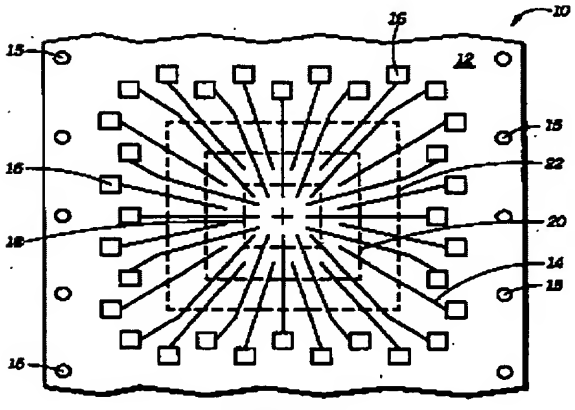

FIG.1

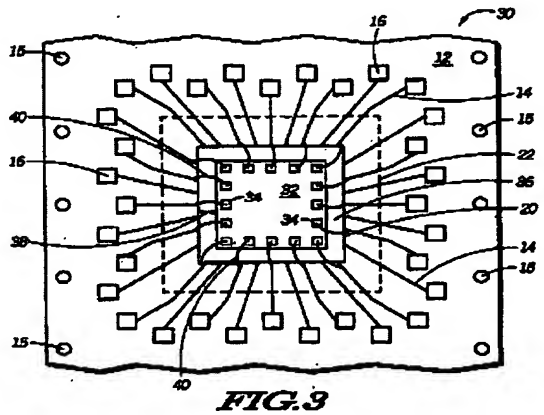

FIG.3

forming a plurality of test pads 16 on the die 30, the plurality of test pads 16 accessible to the testing apparatus, at least one of the plurality of test pads 16 corresponding to at least one of the plurality of input bond pads 34; forming a conductive path 14 between the at least one of the plurality of test pads 16 and the at least one of the plurality of input bond pads 34, wherein a portion of the conductive path 14 is formed on the die 30 between an edge of the die 32 and the active portion 20 of the die 30 (col. 4, lines 10-34 and FIGS. 1 and 3); and testing the die 30 by contacting the at least one of plurality of test pads 16 with the testing apparatus (col. 4, line 65 to col. 5, line 7).

In re claim 2, as applied to claim 1 above, **Higgins** discloses all claimed limitations including the limitation wherein the plurality of test pads 16 is formed on the active portion 20 of the die 30 (col. 4, lines 14-17 and FIG. 3).

In re claim 3, as applied to claim 2 above, **Higgins** discloses all claimed limitations including the limitation wherein the active portion 20 being surrounded by an inactive portion 12, wherein the conductive path extends from the at least one input bond pad 34 to the inactive portion and from the inactive portion 12 to the at least one test pad 16 (col. 3, lines 28-43 and FIG. 3).

In re claim 4, as applied to claim 1 above, **Higgins** discloses all claimed limitations including the limitation wherein portion of the conductive path 14 is formed on wafer outside of the die (FIG. 3).

In re claim 5, as applied to claim 1 above, **Higgins** discloses all claimed limitations including the limitation wherein severing the conductive path 14 at a point outside of the active portion 20 of the die 30 (FIG. 3).

In re claim 6, as applied to claim 3 above, **Higgins** discloses all claimed limitations including the limitation wherein severing the conductive path 14 at a point within the inactive portion 20 (FIG. 3).

In re claim 7, as applied to claim 4 above, **Higgins** discloses all claimed limitations including the limitation wherein severing the conductive path 14 at a point outside the die 30 (FIG. 3).

In re claim 8, as applied to claim 1 above, **Higgins** discloses all claimed limitations including the limitation wherein at least one test pad 16 is of a sufficient size so as to be accessible by a testing apparatus (col. 4, line 65 to col. 5, line 7 and FIG. 3).

In re claim 9, **Higgins** discloses a die assembly formed on a wafer, the die assembly comprising, a die 30 formed on a wafer 10, the die 30 having an active portion 20 comprising integrated circuitry, at least one input bond pad 34 formed on the active portion 20 of the die 30; at least one test pad 16 formed entirely on the die 30 (col. 4, line 65 to col. 5, line 7); and a conductive path 14 that electrically couples the at least one input bond pad 34 to the at least one test pad 16, wherein a portion of the conductive path 14 is formed between an edge of the die 30 and the active portion 20 of the die 30 (col. 4, lines 10-34 and FIGS. 1 and 3).

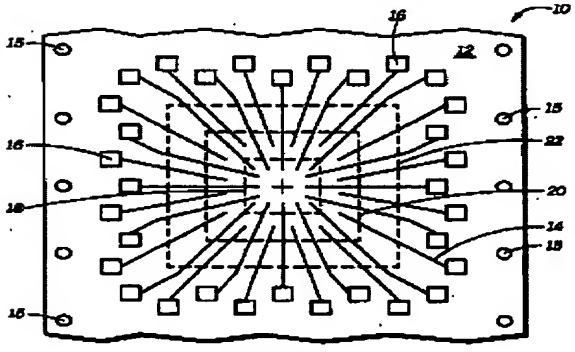

FIG.1

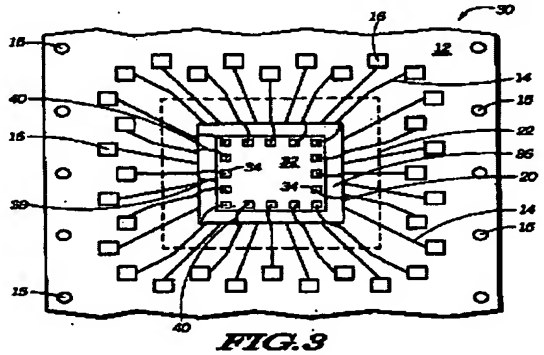

FIG.3

In re claim 10, as applied to claim 9 above, **Higgins** discloses all claimed limitations including the limitation wherein the plurality of test pads 16 is formed on the active portion 20 of the die 30 (col. 4, lines 14-17 and FIG. 3).

In re claim 11, as applied to claim 10 above, **Higgins** discloses all claimed limitations including the limitation wherein the active portion 20 being surrounded by an inactive portion 12, wherein the conductive path extends from the at least one input bond pad 34 to the inactive portion and from the inactive portion 12 to the at least one test pad 16 (col. 3, lines 28-43 and FIG. 3).

In re claim 12, as applied to claim 9 above, **Higgins** discloses all claimed limitations including the limitation wherein the die being surround by a non-conducting scribe area on the wafer 10, wherein the portion of the conductive path 14 is formed on the non-conducting scribe area 12 (FIG. 3).

In re claim 13, as applied to claim 9 above, **Higgins** discloses all claimed limitations including the limitation wherein at least one test pad 16 is of a sufficient size so as to be accessible by a testing apparatus (col. 4, line 65 to col. 5, line 7 and FIG. 3).

In re claim 14, **Higgins** discloses a method for preparing a die on a wafer for testing by a testing apparatus, the method comprising, forming a die 30 on a wafer 10, the die 30 having an active portion 20 comprising integrated circuitry, forming a plurality of input bond pads 34 on the active portion 20; forming a plurality of test pads 16 entirely on the die 30, wherein the plurality of test pads 16 accessible to the testing apparatus (col. 4, line 65 to col. 5, line 7), at least one of the plurality of test pads 16 corresponding to at least one of the plurality of input bond pads 34; forming a conductive path 14 between

the at least one of the plurality of test pads 16 and the at least one of the plurality of input bond pads 34, wherein a portion of the conductive path 14 is formed on the die between an edge of the die 30 and the active portion 20 of the die 30 (col. 4, lines 10-34 and FIGS. 1 and 3); and

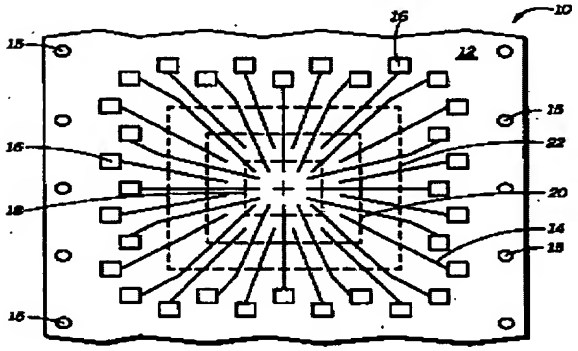

FIG. 1

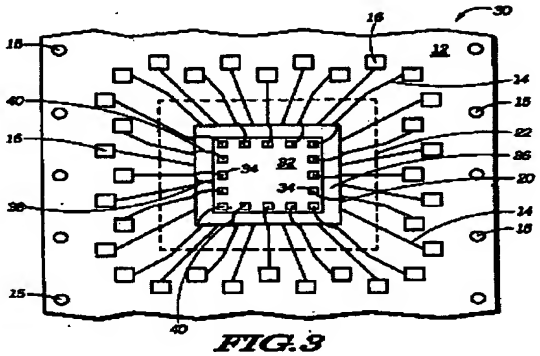

FIG. 3

testing the die 30 by contacting the at least one of plurality of test pads 16 with the testing apparatus (col. 4, line 65 to col. 5, line 7).

In re claim 15, as applied to claim 14 above, **Higgins** discloses all claimed limitations including the limitation wherein the plurality of test pads 16 is formed on the active portion 20 of the die 30 (col. 4, lines 14-17 and FIG. 3).

In re claim 16, as applied to claim 14 above, **Higgins** discloses all claimed limitations including the limitation wherein the active portion 20 being surrounded by an inactive portion 12, wherein the portion of the conductive path 16 is formed on the inactive portion 12 (col. 3, lines 28-43 and FIG. 3).

In re claim 17, as applied to claim 14 above, **Higgins** discloses all claimed limitations including the limitation wherein portion of the conductive path 14 is formed on wafer outside of the die (FIG. 3).

In re claim 18, as applied to claim 14 above, **Higgins** discloses all claimed limitations including the limitation wherein severing the conductive path 14 at a point outside of the active portion 20 of the die 30 (FIG. 3).

In re claim 19, as applied to claim 16 above, **Higgins** discloses all claimed limitations including the limitation wherein severing the conductive path 14 at a point within the inactive portion 20 (FIG. 3).

In re claim 20, as applied to claim 17 above, **Higgins** discloses all claimed limitations including the limitation wherein severing the conductive path 14 at a point outside the die 30 (FIG. 3).

In re claim 21, as applied to claim 14 above, **Higgins** discloses all claimed limitations including the limitation wherein at least one of the plurality of test pad 16 is larger in size than the at least one of the plurality of the input bond pads 34 (col. 4, line 65 to col. 5, line 7 and FIG. 3).

In re claim 22, **Higgins** discloses a die comprising, an active portion 20 comprising integrated circuitry;

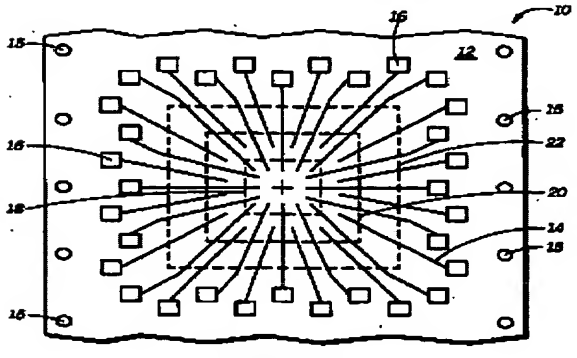

FIG.1

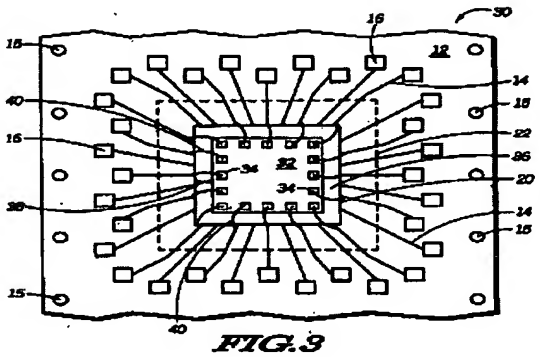

FIG.3

a plurality of input bond pads 34 formed on the active portion 20; a plurality of test pads **20** formed entirely on the die 30, and the plurality of conductive lines 14,

wherein each of the conductive lines 14 is initially formed to electrically couple at least one of the plurality of input bond pads 34 to at least one of the plurality of test pads 16 (col. 4, line 65 to col. 5, line 7), and wherein a portion of each of the conductive lines 14 is formed on an area between an edge of the die 30 and the active portion 20 of the die 30 (col. 4, lines 10-34 and FIGS. 1 and 3).

In re claim 23, as applied to claim 22 above, **Higgins** discloses all claimed limitations including the limitation wherein the plurality of test pads 16 is formed on the active portion 20 of the die 30 (col. 4, lines 14-17 and FIG. 3).

In re claim 24, as applied to claim 22 above, **Higgins** discloses all claimed limitations including the limitation wherein the active portion 20 being surrounded by an inactive portion 12, wherein the conductive path extends from the at least one input bond pad 34 to the inactive portion and from the inactive portion 12 to the at least one test pad 16 (col. 3, lines 28-43 and FIG. 3).

In re claim 25, as applied to claim 22 above, **Higgins** discloses all claimed limitations including the limitation wherein portion of the conductive lines 14 is formed on wafer outside of the die 30 and is subsequently severed at a point outside the die (FIG. 3).

In re claim 26, as applied to claim 25 above, **Higgins** discloses all claimed limitations including the limitation wherein the portion of each of the conductive lines 14 is severed when the die 30 is separated from the wafer (FIG. 3).

In re claim 27, as applied to claim 22 above, **Higgins** discloses all claimed limitations including the limitation wherein the at least one of the plurality of test pads 16 is larger in size than the at least one of the plurality of input bond pads 34(FIG. 3).

In re claim 28, **Higgins** discloses a die comprising, an active portion 20 comprising integrated circuitry, a plurality of input bond pads 34 formed on the active portion 20; a plurality of test pads 16 formed on the die 30 (col. 4, line 65 to col. 5, line 7), a plurality of conductive lines 14, wherein each of the conductive lines 14 is initially formed to electrically couple the at least one of the plurality of input bond pad 34 to the at least one of the plurality of test pad 16, and wherein a portion of each of the conductive lines 14 is formed on a scribe area outside the die 30 (col. 4, lines 10-34 and FIGS. 1 and 3).

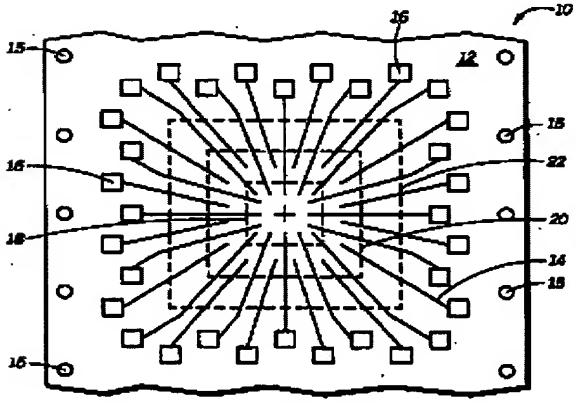

FIG.1

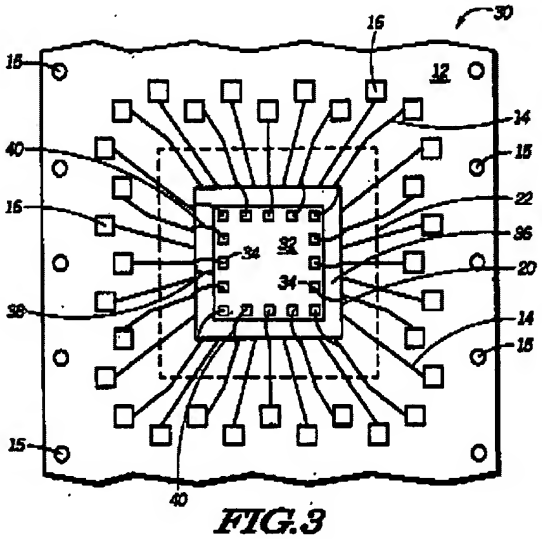

FIG.3

Response to Applicant's Amendment and Argument

4. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER

K.N.
August 10, 2006